Claims

What is claimed is:

1. A 5B/6B encoder suitable for operating on source vectors having five source bits, the encoder operative to translate the source vectors from a plurality of source vectors into six-bit coded vectors by appending a sixth bit having a default value to the source vectors and by complementation of selected one to three individual source bits for a minority of the plurality of source vectors, wherein the coded vectors are disparity independent with a single representation or disparity dependent with a primary and an alternate representation, and wherein the alternate representation is a complement of the primary representation.

2. An encoder according to claim 1, wherein the minority of source vectors comprises less than half of the plurality of source vectors.

3. An encoder according to claim 2, wherein the minority of source vectors comprises nine source vectors, wherein there are 33 source vectors in the plurality of source vectors, and wherein there are 33 coded primary vectors in the plurality of coded vectors.

4. An encoder according to claim 1, further comprising a control input, the encoder further operative to generate, when the control input is asserted in parallel with a given data vector, an additional coded vector with a trailing run length different from trailing run lengths of all of the other coded vectors.

5. An encoder according to claim 1, wherein the encoder is further operative to generate nine disparity independent coded vectors and 15 disparity dependent primary coded vectors solely by appending a bit with a specified default value to selected source vectors.

6. An encoder according to claim 1, wherein the encoder is further operative to generate nine disparity independent balanced coded vectors by appending a bit with a default value and complementation of one to three source bits for selected source vectors.

7. An encoder according to claim 5, wherein the appended bit has a value of zero and wherein the encoder is further operative to generate the nine disparity independent balanced coded vectors from a set of source vectors that have a disparity of plus one and no more than one trailing zero.

8. An encoder according to claim 5, wherein the appended bit has a value of zero, wherein one of the disparity dependent primary coded vectors is balanced, and wherein the encoder is further operative to generate the one balanced disparity dependent primary coded vector from a source vector having a disparity of plus one and three leading ones.

9. An encoder according to claim 5, wherein the appended bit has a value of zero, wherein four of the disparity dependent primary coded vectors have a disparity of plus two, and wherein the encoder is further operative to generate the four disparity dependent primary coded vectors from source vectors having a disparity of plus three and one trailing one.

10. An encoder according to claim 5, wherein the appended bit has a value of zero, wherein ten of the disparity dependent primary coded vectors have a disparity of minus two, and wherein the encoder is further operative to generate the ten disparity dependent primary coded vectors from source vectors with a disparity of minus one.

11. An encoder according to claim 6, wherein the appended bit has a value of one, wherein the nine disparity independent coded vectors are balanced, and wherein the encoder is further operative to generate the nine balanced disparity independent coded vectors from a set of source vectors with a disparity of minus one and no more than one trailing one.

12. A method for translating source vectors having five source bits into six-bit coded vectors, wherein each source vector is selected from a plurality of source vectors, the method comprising the steps of:

appending a sixth bit having a default value to the source vectors; and

complementing selected one to three individual source bits for a minority of the plurality of source vectors;

wherein the coded vectors are disparity independent with a single representation or disparity dependent with a primary and an alternate representation, and wherein the alternate representation is a complement of the primary representation.

13. A 3B/4B encoder suitable for operating on source vectors having three source bits, the source vectors from a plurality of source vectors, the encoder operative to translate source vectors, together with one or more control inputs, into one of nine four-bit coded vectors by appending a fourth bit having a default value to the source vectors and by complementing a single individual source bit for a minority of the plurality of source vectors, wherein the coded vectors are disparity independent with a single representation or disparity dependent with a primary and an alternate representation, and wherein the alternate representation is a complement of the primary representation.

14. An encoder according to claim 13, further operative to assign a second primary coded vector to a source vector of '111,' wherein the encoder assigns the second primary coded vector only when a first primary coded vector would generate a false comma sequence or when a given one of the one or more control inputs is asserted.

15. An encoder according to claim 14, wherein the encoder is further operative, when determining a coded vector corresponding to a given source vector, to set the appended bit to a value of one if two trailing source bits in the given source vector are both zero or if the second primary coded vector is to be encoded.

16. An encoder according to claim 14, wherein the encoder is further operative, when determining a given coded vector corresponding to a given source vector, to set the appended bit to a value of zero for the given coded vector if at least one of two trailing source bits in the source vector is a one and if the second primary vector is not to be encoded.

17. An encoder according to claim 13, wherein the encoder is further operative, when determining a given coded vector corresponding to a given source vector, to complement a second bit in the given source vector to one if all three source bits in the given source vector have a value of zero.

18. An encoder according to claim 14, wherein the encoder is further operative, when determining a coded vector corresponding to a given source vector, to complement the first source bit to zero in the given source vector if the second primary vector is to be encoded.

19. An encoder according to claim 13, wherein the encoder is further operative to complement four primary coded vectors which are balanced and otherwise disparity independent if a running disparity is positive and a given one of the one or more control inputs is asserted.

20. A method for translating source vectors having three source bits into four-bit coded vectors, wherein each source vector is selected from a plurality of source vectors, the method translating source vectors, together with one or more control inputs, into one of nine four-bit coded vectors, the method comprising the steps of:

appending a fourth bit having a default value to the source vectors; and

complementing a single individual source bit for a minority of source vectors,

wherein the coded vectors are disparity independent with a single representation or disparity dependent with a primary and an alternate representation, and wherein the alternate representation is a complement of the primary representation.

21. A partitioned 8B/10B encoder comprising:

at least one control input;

a 3B/4B encoder, coupled to the at least one control input, suitable for operating on three-bit source vectors having three source bits, the three-bit source vectors from a plurality of three-bit source vectors, the 3B/4B encoder operative to translate three-bit source vectors, together with information from the at least one control input, into one of nine four-bit coded vectors by appending a fourth bit with a default value and by complementing a single individual

source bit for a minority of three-bit source vectors, wherein the four-bit coded vectors are disparity independent with a single representation or disparity dependent with a primary and an alternate representation, wherein the alternate representation is a complement of the primary representation, wherein the 3B/4B encoder is further operative to assign a second primary four-bit coded vector to a three-bit source vector of '111,' and wherein the 3B/4B encoder assigns the second primary four-bit coded vector only when a first primary four-bit coded vector would generate a false comma sequence or when the at least one control input is asserted; and

a 5B/6B encoder, coupled to the 3B/4B encoder and the at least one control input, suitable for operating on five-bit source vectors, each having five source bits, the five-bit source vectors from a plurality of five-bit source vectors, the 5B/6B encoder operative to translate five-bit source vectors from a plurality of five-bit source vectors into six-bit coded vectors by appending a sixth bit having a default value to the five-bit source vectors and by complementation of selected one to three individual source bits for a minority of the plurality of five-bit source vectors, wherein the six-bit coded vectors are disparity independent with a single representation or disparity dependent with a primary and an alternate representation;

wherein the 8B/10B encoder is operative to determine a set of control characters by using the second primary four-bit coded vector in situations that do not require the second primary four-bit coded vector for false comma avoidance in combination with selected balanced six-bit coded vectors that are made disparity dependent in response to at least one asserted control input of the at least one control inputs.

22. A 10B/12B encoder for a partitioned 10B/12B transmission code, the 10B/12B encoder comprising a pair of 5B/6B encoders, each of which operates on five-bit source vectors to produce six-bit coded vectors, the 10B/12B encoder operative:

to determine a starting disparity;

to generate a synchronizing coded pattern based on the starting disparity, wherein when the starting disparity is positive a predetermined pattern is generated or when the starting disparity is negative a complement of the predetermined pattern is generated.

23. The 10B/12B encoder of claim 22, wherein the predetermined pattern is '110000 010011'.

24. A 10B/12B encoder according to claim 22, wherein the 10B/12B encoder is operative to generate a first set of control characters, the control characters in the first set being characterized a first leading and first trailing coded vector and by a trailing run of 4 in the first leading coded vector followed by the first trailing code vector that is one of 13 unbalanced coded vectors or one of 15 balanced vectors that do not generate a run of six when following the first leading coded vector.

25. The 10B/12B encoder according to claim 24, wherein the 10B/12B encoder is further operative to generate a second set of control characters, the control characters in the second set characterized by second leading and second trailing coded vectors and by a leading run of 4 in the second trailing coded vector, preceded by a second leading coded vector that is one of 13 unbalanced coded vectors or one of 15 balanced vectors that do not generate a run of six when preceding a run of four occurs in the second leading coded vector.

26. A 10B/12B encoder according to claim 25, wherein the 10B/12B encoder comprises a control input and wherein the balanced vectors are made disparity dependent when the control input is asserted.

27. A method for synchronizing a partitioned 10B/12B transmission code, the partitioned 10B/12B transmission code using two five-bit source vectors to produce two six-bit coded vectors, the method comprising the steps of:

determining a starting disparity; and

generating a synchronizing coded pattern based on the starting disparity, wherein when the starting disparity is positive a predetermined pattern is generated or when the starting disparity is negative a complement of the predetermined pattern is generated.